	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	4	wang near chia-chung.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/23 16:19	
2	BRS	L2	106	lin near charles.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/23 16:27	
3	BRS	L3	5243	(semiconductor) near35 (trace)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/23 16:28	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
4	BRS	L4	1403	(semiconductor) near35 (conductive near trace)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/23 16:29	
5	BRS	L5	526	(semiconductor) near35 (conductive near trace) near35 (pad)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/23 16:29	
6	BRS	L6	122	(semiconductor) near35 (conductive near trace) near35 (pad) near50 (cavity or recess or opening or hole or aperture)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/23 16:59	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
7	BRS	L7	515	(conductive near trace) near35 (pad) near50 (cavity or recess or opening or hole or aperture)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/23 17:00	
8	BRS	L8	4114	(chip or die or device) near35 (trace) near35 (substrate or wafer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/23 17:36	
9	BRS	L9	1671	(chip or die or device) near35 (conductive near trace) near35 (substrate or wafer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/23 17:37	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
10	BRS	L10	231	(chip or die or device) near35 (conductive near trace) near35 (substrate or wafer) near50 (hole or aperture or cavity or recess or opening)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/23 17:37	
11	BRS	L12	12	(chip or die or device) near35 (conductive near trace) near35 (substrate or wafer) near50 (hole or aperture or cavity or recess or opening) near35 (pad$1) near35 (terminal$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/23 17:38	
12	BRS	L11	99	(chip or die or device) near35 (conductive near trace) near35 (substrate or wafer) near50 (hole or aperture or cavity or recess or opening) near35 (pad$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/23 17:39	

	U	1	Document ID	Title	Current OR	Pages
1	☒	☐	US 20040159957 A1	Interposer substrate and wafer scale interposer substrate member for use with flip-chip configured semiconductor dice	257/778	32
2	☒	☐	US 20030166312 A1	Methods for assembly and packaging of flip chip configured dice with interposer	438/107	27
3	☒	☐	US 20030164548 A1	Flip chip packaging using recessed interposer terminals	257/738	29
4	☒	☐	US 20030164541 A1	Method and apparatus for dielectric filling of flip chip on interposer assembly	257/686	34
5	☒	☐	US 20020079593 A1	Semiconductor package having heat sink attached to substrate	257/778	8
6	☐	☐	US 6528876 B2	Semiconductor package having heat sink attached to substrate	257/706	8
7	☐	☐	US 6475833 B2	Bumpless flip chip assembly with strips and via-fill	438/121	16
8	☐	☐	US 6437452 B2	Bumpless flip chip assembly with strips-in-via and plating	257/784	18

	U	1	Document ID	Title	Current OR	Pages
9	☐	☐	US 6403400 B2	Bumpless flip chip assembly with strips-in-via and plating	438/121	19
10	☐	☐	US 6316830 B1	Bumpless flip chip assembly with strips and via-fill	257/737	13
11	☐	☐	US 5981873 A	Printed circuit board for ball grid array semiconductor package	174/52.2	10
12	☐	☐	US 6316830 B	Flip chip assembly for ball grid array package, includes electrically conductive material in through-holes on dielectric substrate, for electrically connecting conductive traces to terminal pads		13